ECED2200 – Digital Circuits

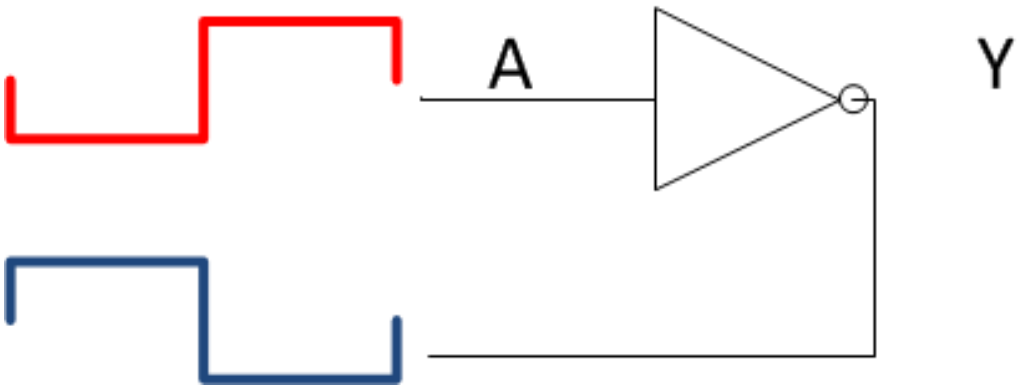
Time Response & Hazards

General Notes

- See updates to these slides: www.newae.com/teaching
- These slides licensed under 'Creative Commons Attribution-ShareAlike 3.0 Unported License'
- These slides are not the complete course – they are extended in-class
- You will find the following references useful, see www.newae.com/teaching for more information/links:
  - The book "Bebop to the Boolean Boogie" which is available to Dalhousie Students
  - Course notes (covers almost everything we will discuss in class)
  - Various websites such as e.g.: www.play-hookey.com
  - The book "Contemporary Logic Design", which was used in previous iterations of the class and you may have already

Time Response of Gates

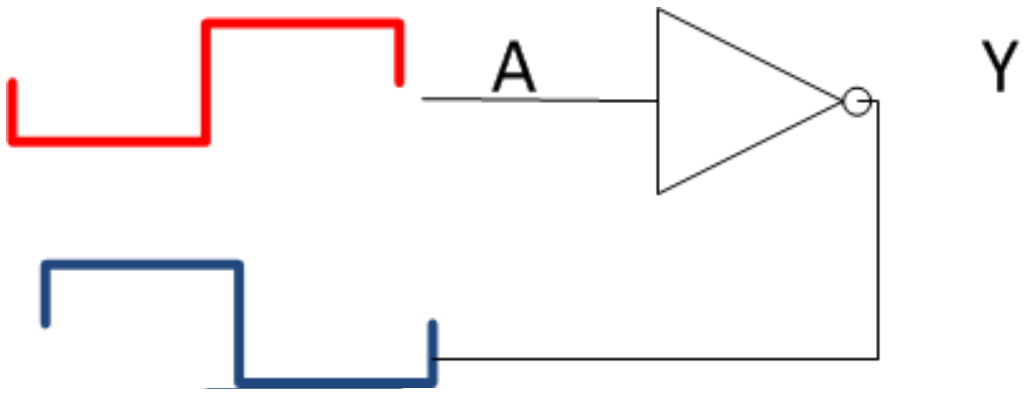
NOT Gate



$$Y = \overline{A}$$

A	Y
0	1
1	0

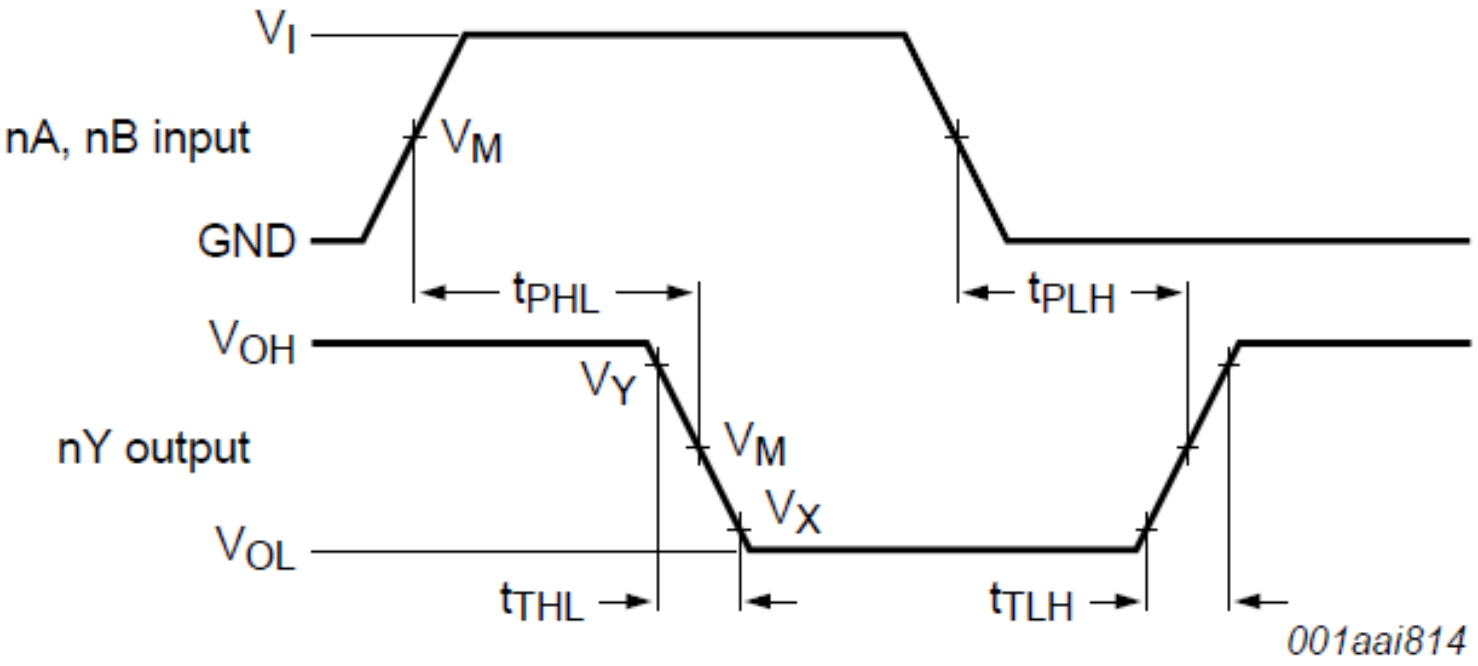
NOT Gate



$$Y = \overline{A}$$

A	Y
0	1
1	0

Time Response



Source: http://www.nxp.com/documents/data_sheet/74HC_HCT00.pdf

Typical Values

74F00:

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		V_{CC} = +5.0V ± 10% T_{amb} = –40°C to +85°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dna, Dnb to $\overline{Q}$n	Waveform 1	2.4 2.0	3.7 3.2	5.0 4.3	2.4 2.0	6.0 5.3	2.0 1.5	6.5 6.0	ns

74HC00:

t_{pd}	propagation delay	nA, nB to nY; see Figure 6	[1]						
		V_{CC} = 2.0 V	-	25	-	115	135	ns	
		V_{CC} = 4.5 V	-	9	-	23	27	ns	
		V_{CC} = 5.0 V; C_L = 15 pF	-	7	-	-	-	ns	

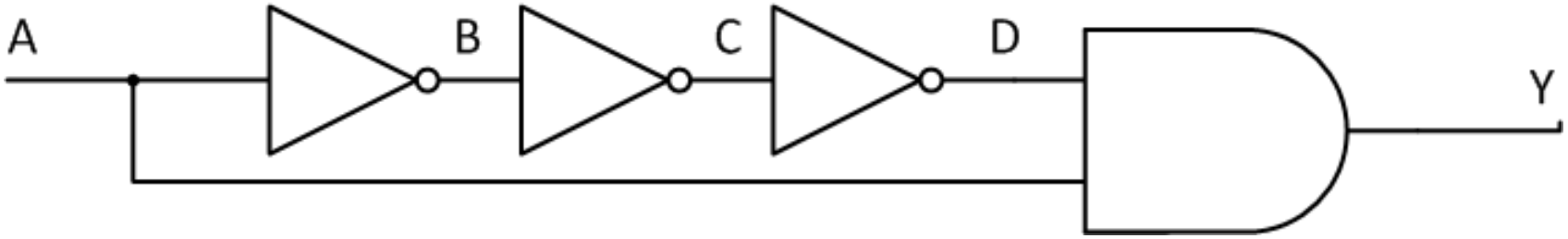
74LS00:

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_{PLH}	Turn-Off Delay, Input to Output		9.0	15	ns	V_{CC} = 5.0 V C_L = 15 pF
t_{PHL}	Turn-On Delay, Input to Output		10	15	ns	

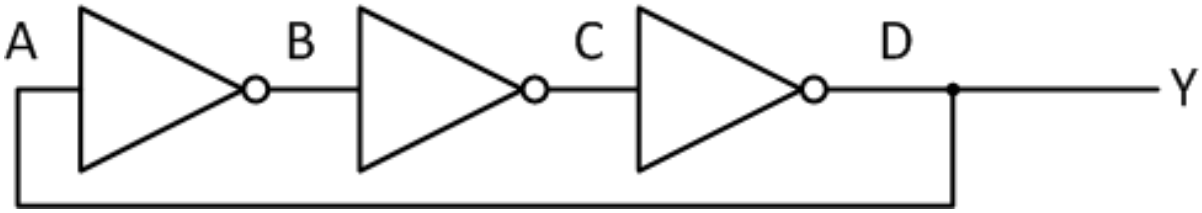
USEFUL GATE DELAYS

Pulse Shaper



A									
B									
C									
D									
Y									

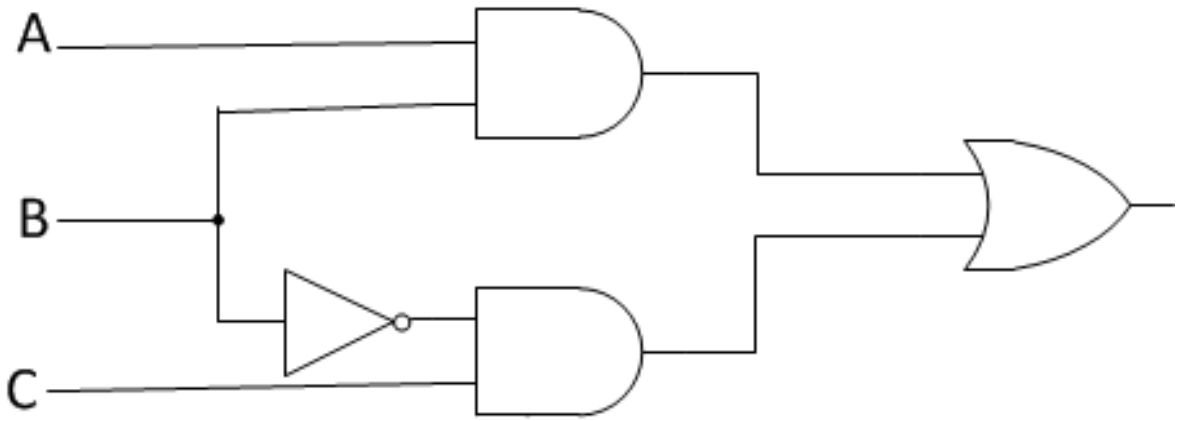
Ring Oscillator



A									
B									
C									
D									
Y									

NOT-SO-USEFUL GATE DELAYS

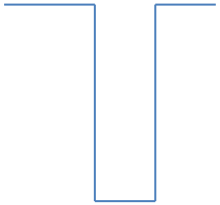
Glitches



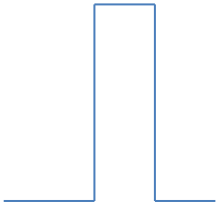
Hazards

- Circuits with *potential for a glitch* have a hazard

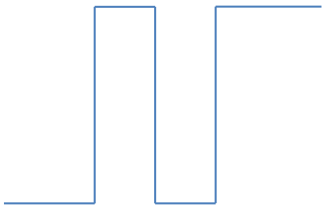
Types of Hazards



Static 1-Hazard



Static 0-Hazard



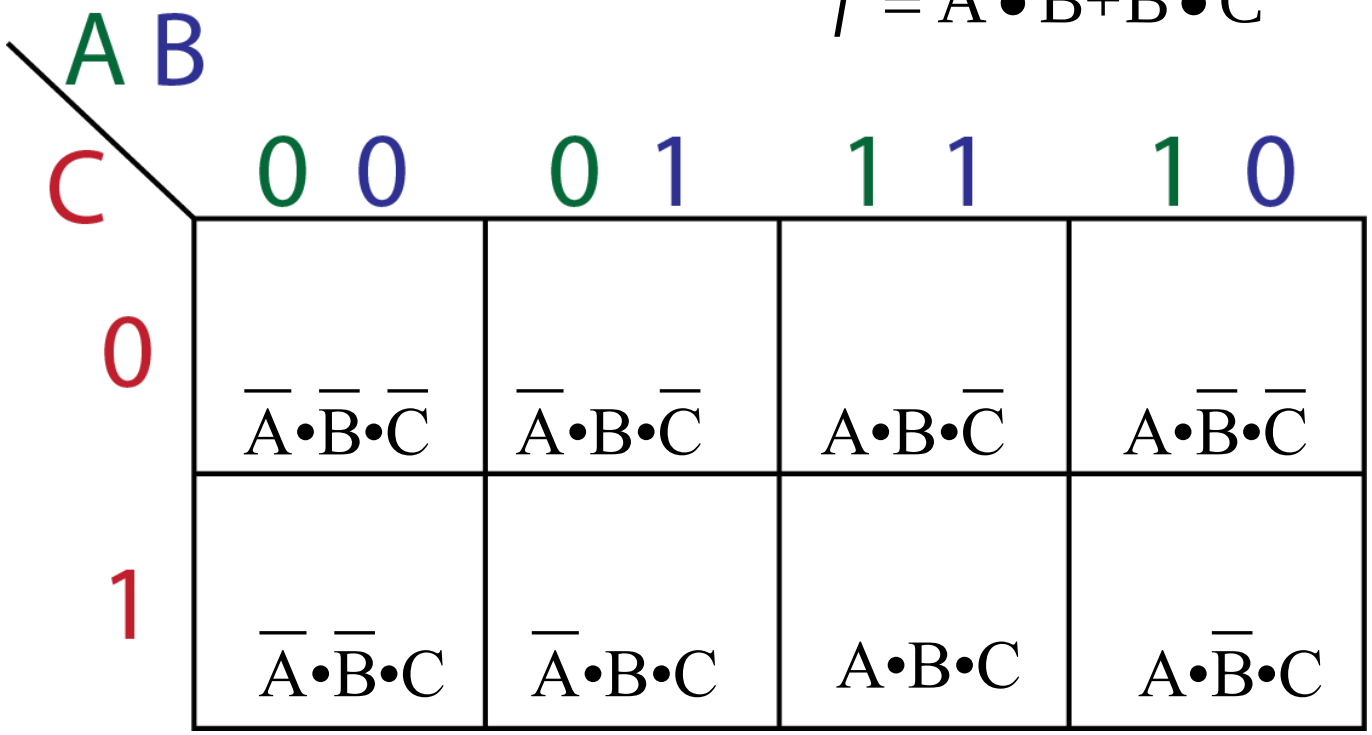
Dynamic Hazard

What Creates Hazards?

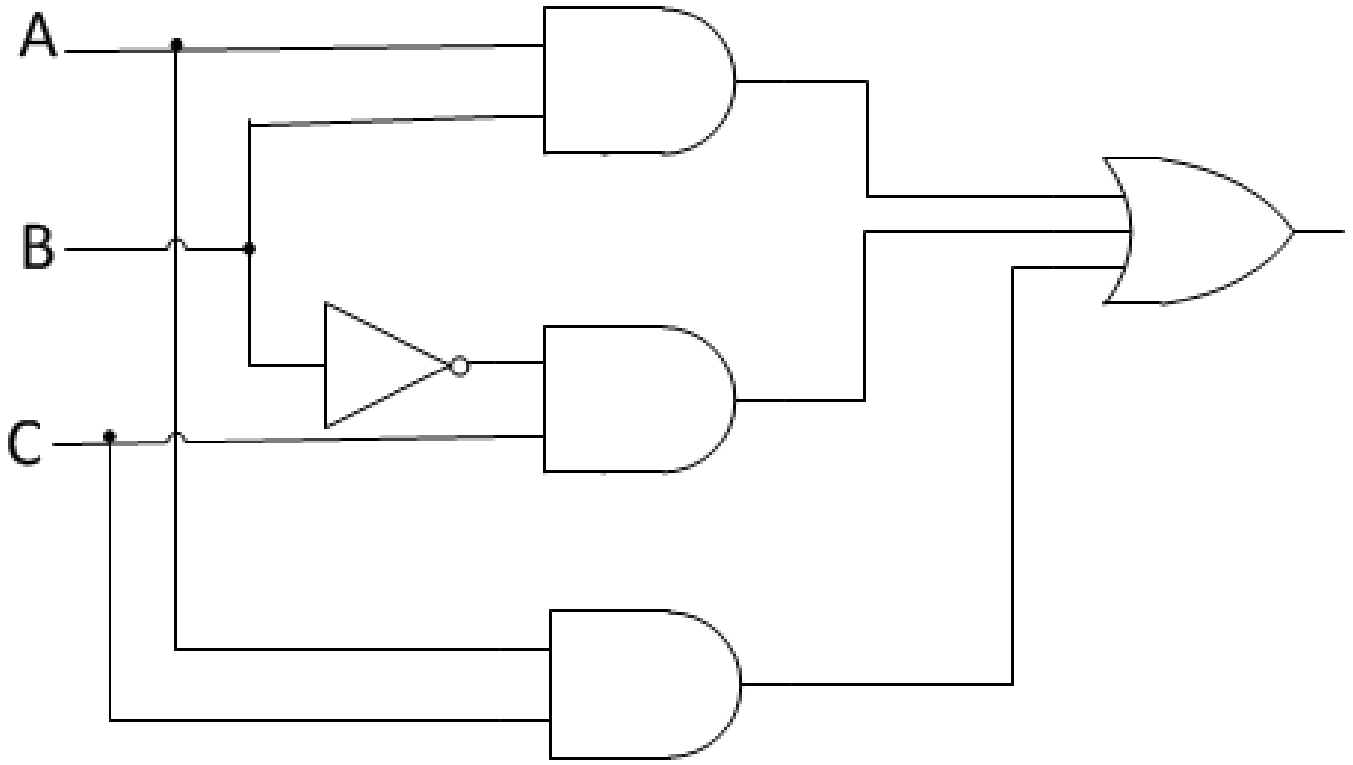
- Single-bit (variable) input changes only!

Analyzing Hazards & Fixing Them

$$f = A \bullet B + \overline{B} \bullet C$$



Hazard Free Form



Other Hazards?

In two-level networks (assuming complements are available) synthesized in sum-of-product form, removal of state 1-hazard means static 0-hazards and dynamic hazards also removed.

Multilevel Hazards

1. Simplify using some basic Boolean laws to get to two-level form
   - CANNOT use complement laws or simplification laws derived from it
2. Using K-Map derive hazard-free form
3. Do not convert back into multilevel form – difficult to remove dynamic hazards

Example

$$f=A \bullet B \bullet C+(A+D) \bullet (\overline{A}+\overline{C})$$

$$f=A \bullet B \bullet C+A \bullet \overline{A}+A \bullet \overline{C}+D \bullet \overline{A}+D \bullet \overline{C}$$

Example

$$f=A\bullet B\bullet C+A\bullet\overline{A}+A\bullet\overline{C}+D\bullet\overline{A}+D\bullet\overline{C}$$

C D \ A B	0 0	0 1	1 1	1 0
0 0	$\overline{A}\bullet\overline{B}\bullet\overline{C}\bullet\overline{D}$	$\overline{A}\bullet B\bullet\overline{C}\bullet\overline{D}$	$A\bullet B\bullet\overline{C}\bullet\overline{D}$	$A\bullet\overline{B}\bullet\overline{C}\bullet\overline{D}$
0 1	$\overline{A}\bullet\overline{B}\bullet\overline{C}\bullet D$	$\overline{A}\bullet B\bullet\overline{C}\bullet D$	$A\bullet B\bullet\overline{C}\bullet D$	$A\bullet\overline{B}\bullet\overline{C}\bullet D$
1 1	$\overline{A}\bullet\overline{B}\bullet C\bullet D$	$\overline{A}\bullet B\bullet C\bullet D$	$A\bullet B\bullet C\bullet D$	$A\bullet\overline{B}\bullet C\bullet D$
1 0	$\overline{A}\bullet\overline{B}\bullet C\bullet\overline{D}$	$\overline{A}\bullet B\bullet C\bullet\overline{D}$	$A\bullet B\bullet C\bullet\overline{D}$	$A\bullet\overline{B}\bullet C\bullet\overline{D}$

References

See class notes “Hazards”